CLAIMS

1. (Original) An apparatus comprising:

a plurality of processing elements each having an addressing space;

a plurality of communication registers shared by and mapped to the addressing space of each processing element of the plurality of processing elements, wherein each of the plurality of communication registers couples a first of the plurality of processing elements to every other one of the plurality of processing elements; and

a write control circuit to write data to a selected communication register, the data to be stored in the selected communication register and to be read by at least one processing element.

2. (Original) The apparatus of claim 1, wherein each communication register of the plurality comprises a data payload field and a data valid field to indicate a target for a data payload.

3. (Original) The apparatus of claim 2, further comprising:

a read control circuit to provide read access to data stored in the selected communication register to at least one selected processing element identified by the data valid field.

4. (Original) The apparatus of claim 3, wherein the read control circuit further comprises:

a decode circuit to decode the data valid field and to provide read access to data stored in the selected communication register to a first of the plurality of processing elements, if the decoded data valid field corresponds to the first of the plurality of processing elements.

5. (Original) The apparatus of claim 3, wherein the read control circuit further comprises:

a deselect circuit to modify the data valid field of the data stored in the selected communication register.

6. (Original) The apparatus of claim 2, wherein the data valid field has a plurality bit locations each corresponding to a potential target of the plurality of processing elements.

7. (Original) The apparatus of claim 6, wherein the target for a data payload is to be indicated by at least one set data valid bit in one of the plurality of bit locations in the data valid field.

8. (Original) The apparatus of claim 7, wherein a first of the processing elements is to set a first of the at least one set data valid bits, and a second of the processing elements is to read the data to be stored, if the first of the at least one set data valid bit is in a potential target register corresponding to the second of the processing elements.

9. (Original) The apparatus of claim 8, further comprising:

a reset circuit to reset the first of the at least one set data valid bits, if a data valid reset signal is received from the second of the processing elements, the data valid reset signal to indicate that the second of the processing elements has completed reading the data to be stored.

10. (Original) The apparatus of claim 2, wherein the write control circuit further comprises:

a communication register selection circuit to identify the selected communication register from a write address signal asserted by one of the plurality of processing elements.

11. (Original) The apparatus of claim 2, wherein each data payload field includes a plurality of bits of data, and each data valid field includes a plurality of data valid bits to indicate a target for the data payload.

12. (Original) The apparatus of claim 3, wherein the write control circuit further comprises:

a stall signal generator to generate a stall signal to stop the plurality of processing elements from writing a second data to the selected communication register, if the data valid field includes a selected processing element.

13. (Original) The apparatus of claim 12, wherein the data write stall signal has a plurality of stall bits, each of the stall bits corresponding to one of the plurality of communication registers, wherein the stall bits have at least one set stall bit identifying the selected communication register that will not accept data from the plurality of processing elements.

14. (Withdrawn) A system comprising:

a plurality of image signal processors (ISPs), each of the ISPs coupled to at least two other of the ISPs, each of the ISPs including a plurality of communication registers and a plurality of processing elements;

a random access memory coupled to at least one of the plurality of ISPs; and

wherein each of the plurality of communication registers is mapped directly to an address space of each processing element of the plurality.

15. (Withdrawn) The system of claim 14, wherein a first of the plurality of processing elements is a memory command handler to read and write data between the plurality of communication registers and a second memory, and a second of the plurality of processing elements is a plurality of hardwired accelerators.

16. (Withdrawn) The system of claim 14, further comprising a write control circuit to write data to a selected communication register, the data to be stored in the selected communication register and to be read by at least one selected processing element.

17. (Previously Presented) A method comprising:

indicating at least one selected processing element of a plurality of processing elements to read data to be written to a selected communication register of a plurality of communication registers;

writing the data to the selected communication register; and

providing access to the data to the selected processing elements.

18. (Previously Presented) The method of claim 17, further comprising:
the selected processing elements reading the data.

19. (Original) The method of claim 17, wherein writing comprises:
writing the data to an address defined within the writing processing elements addressing space that maps directly to the selected communication register.

20. (Original) The method of claim 17, wherein indicating includes setting at least one of a plurality of data valid bits in the data to be written, each of the plurality of data valid bits corresponding to one of the plurality of processing elements, the set data valid bits identifying the at least one selected processing element.

21. (Previously Presented) The method of claim 20, further comprising:
the selected processing elements reading the data, if the data has a set data valid bit identifying the selected processing elements.

22. (Previously Presented) The method of claim 20, wherein a first of the processing elements sets the set data valid bits, and a second of the processing elements reads the data, if one of the set data valid bits of the stored data identifies the second of the processing elements.

23. (Previously Presented) The method of claim 22, further comprising:
the second of the processing elements returning a data valid reset signal to the selected communication register, if the second of the processing elements has completed reading the data; and
resetting the one of the set data valid bits of the data identifying the second of the processing elements.

24. (Previously Presented) The method of claim 20, further comprising asserting a data write stall signal to the plurality of processing elements to stop the plurality of

processing elements from writing a second data to the selected communication register, if the data includes a set data valid bit.

25. (Previously Presented) The method of claim 20, further comprising writing a second data to the selected communication register, if the data does not include a set data valid bit.

26. (Previously Presented) The method of claim 17, wherein providing access further comprises:

broadcasting the data to the address defined within the writing processing elements addressing space of each of the processing elements.